Design and Productization of Highly-Integrated Low-Cost Mixed-Signal SoCs

Course Outline

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Overview

- **The course focuses primarily on system-level design considerations for highly integrated mixed-signal SoCs**
- **Emphasis on productization aspects and how these impact the design**
  - **transceiver architecture considerations**
  - **built in characterization and production-testing**
  - **self-interference problems and solutions**
- **Defining and interpreting performance specifications**
- **Designing for testability**
- **Built-in calibration/compensation (“self healing”)**

Background

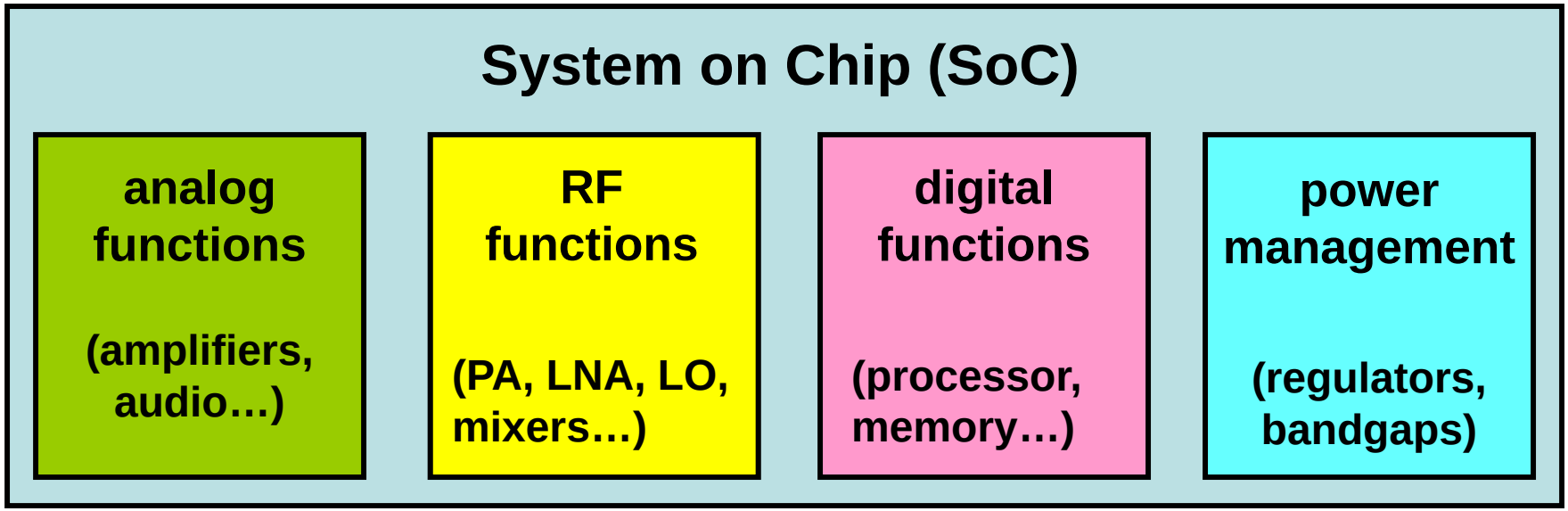
- **The course material is based primarily on design and productization experience from TI's Wireless Terminals Business Unit (WTBU)**

- **The presented concepts have been demonstrated in multiple successful RF SoC products**
- **The presented approaches are critical in achieving the much needed cost-competitiveness of the consumer market**

Example Slides

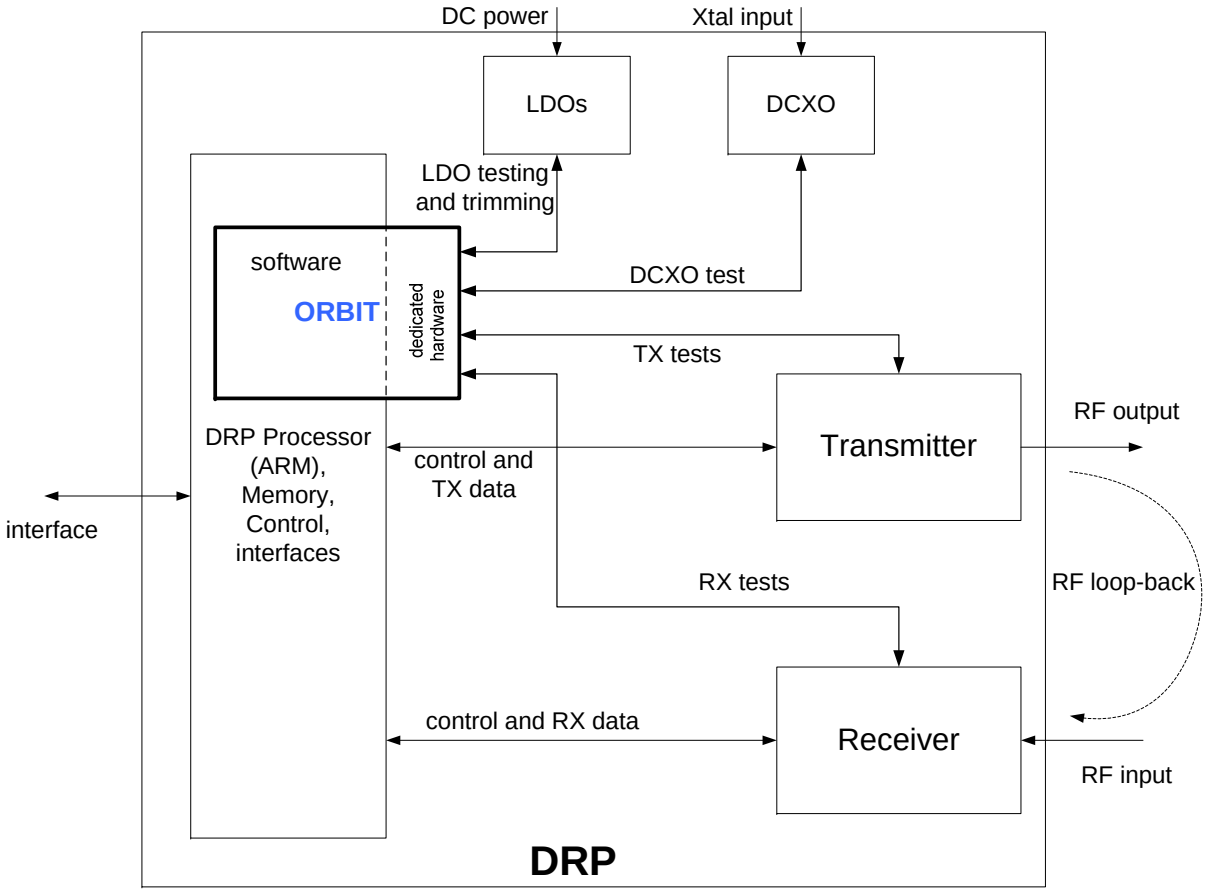
Self-Interference in Complex SoCs

- Aggressive cost and size targets are driving ever increasing levels of integration
- A typical transceiver CMOS system-on-chip (SoC) may include not only a digital processor and the RF transceiver, but even multiple radios (e.g., Bluetooth + WLAN + FM).
- The potential for self-interference in the SoC grows exponentially with the increase in complexity and integration.



Built-in Self-Testing of Transceivers

- Eliminate the need for expensive RF testers
  - generate internal stimuli
  - evaluate signals internally through digital signal processing
- Defect-oriented testing instead of parametric
  - Allows crude measurements instead of accurate (e.g., loopback)
  - relies on the assumption that the design is robust (digitally compensated and does not suffer marginalities)



A statistical approach to high-yield design

- Statistical distribution of performance is narrowed using calibration/compensation